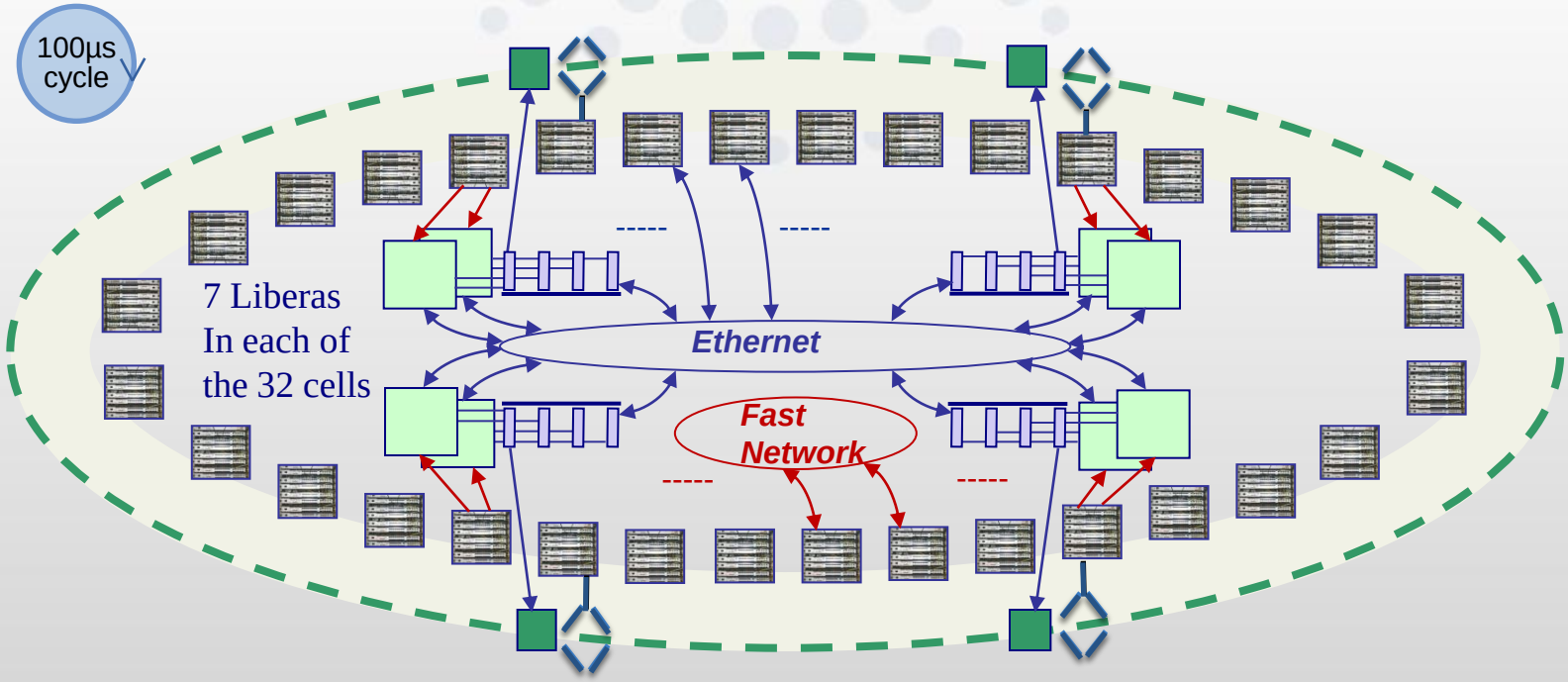
ESRF Fast Orbit Feedback

Upgrade

- *Topology & Sequencing*
- *Material involved- Development tools*
- *Loop latency*
- *Planning*

ESRF Fast Orbit Feedback

Fast Orbit Feedback sequencing → ***1: Beam position acquisition on 224 Libera BPMs***



One of the 224 Beam Position Monitors

Group of 7 Libera BPMs per cell

4 cabinets of 18 corrector's channels each

One of the 8 Feedback Processors

One of the 96 sextupoles housing the correctors

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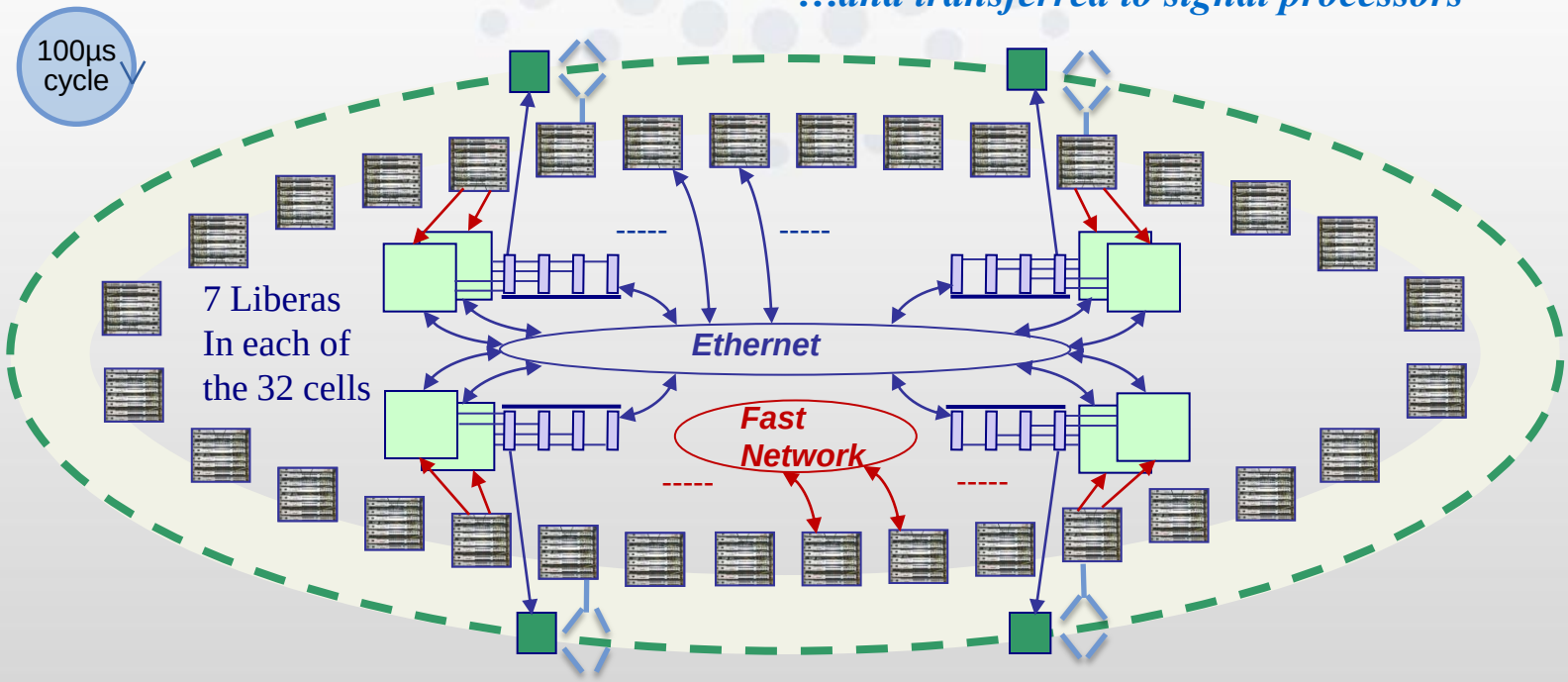
Fast Orbit Feedback sequencing → *2: All positions exchanged between Liberas…*
…and transferred to signal processors



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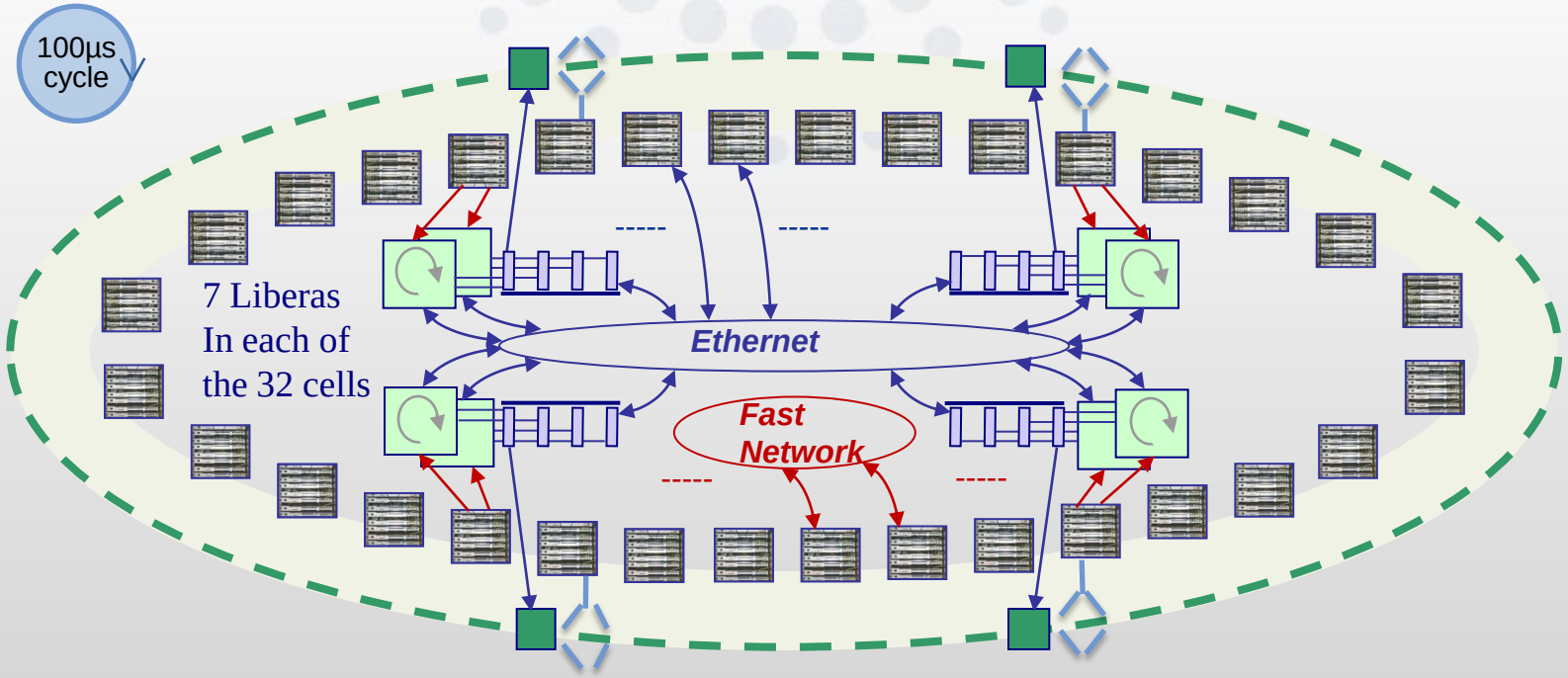
Fast Orbit Feedback sequencing → ***3: Corrections computation on 8 stations (FPGAs)***



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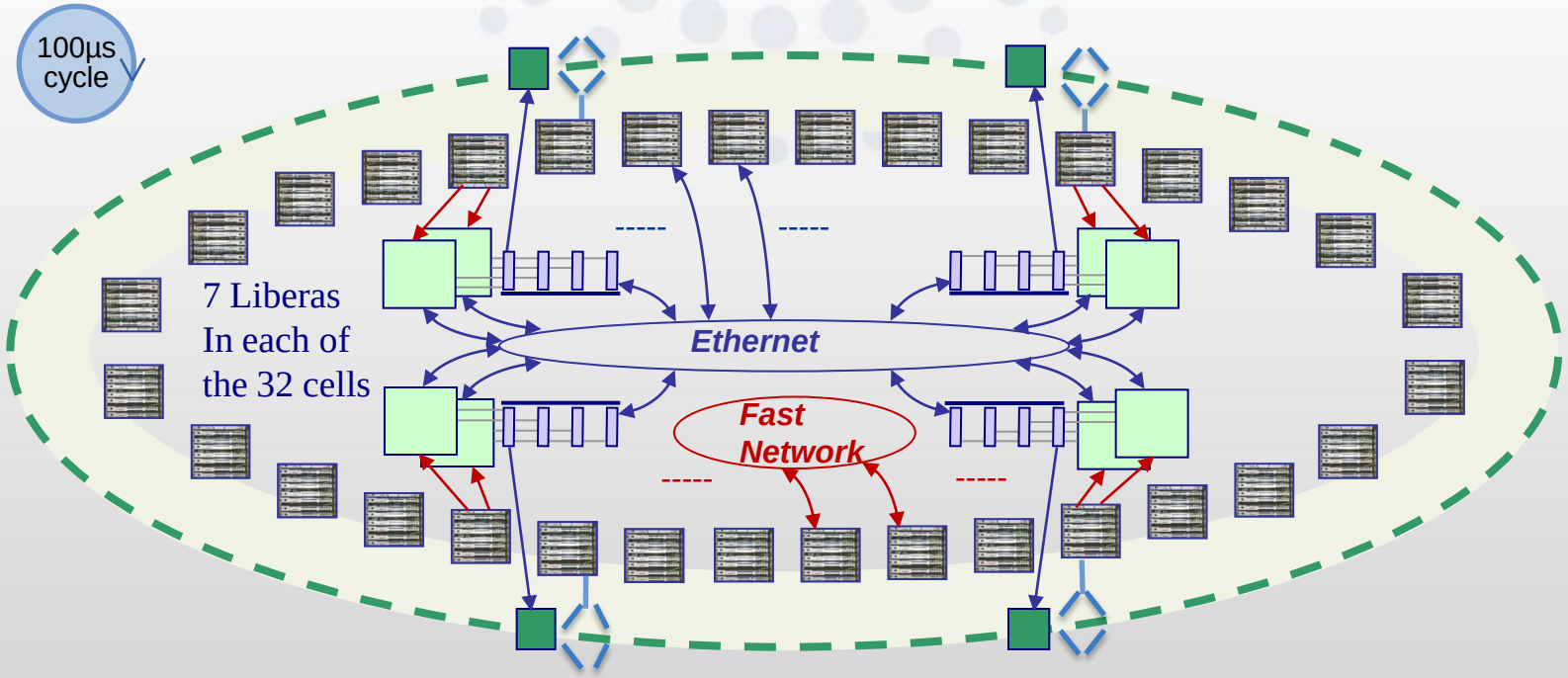
Fast Orbit Feedback sequencing → ***4: Corrections transferred to Power Converters***



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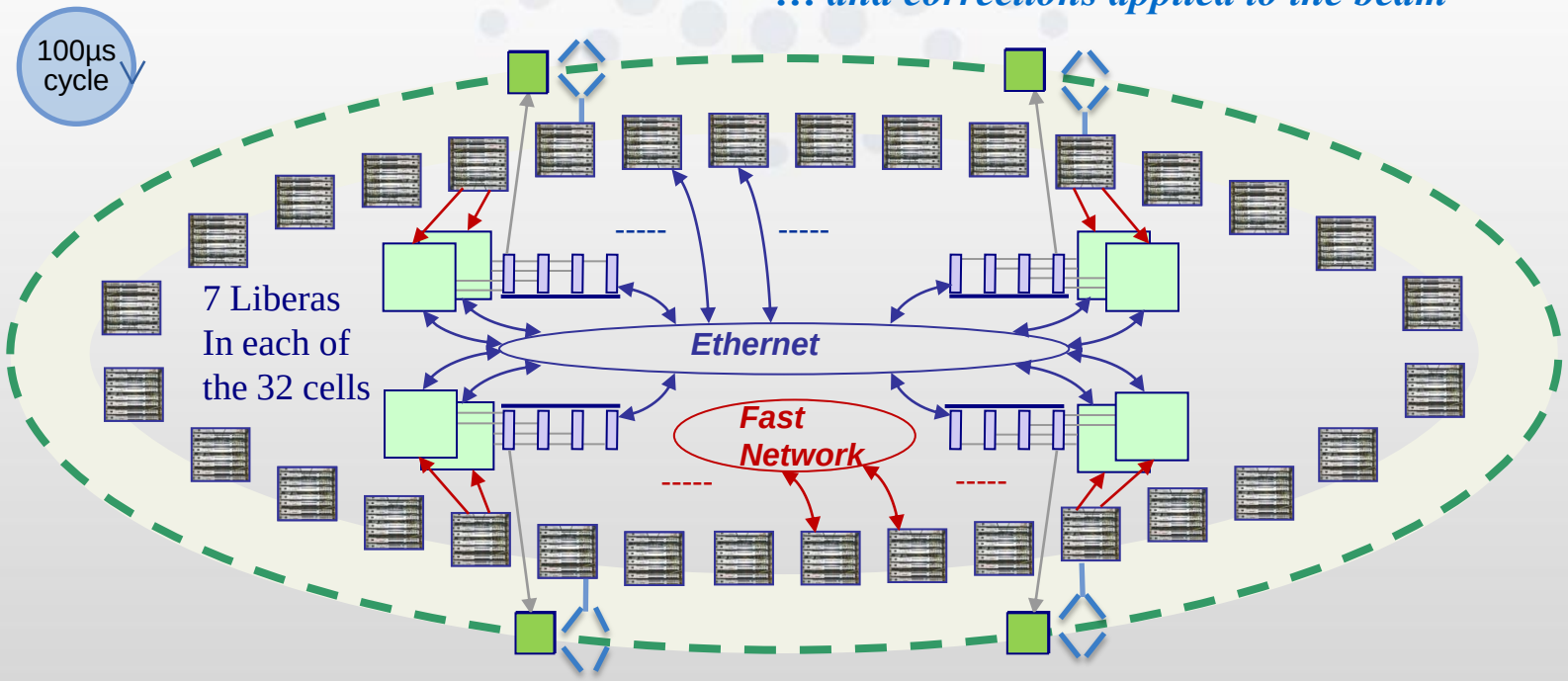
Fast Orbit Feedback sequencing → *5: Current sent to the correctors…*
… and corrections applied to the beam



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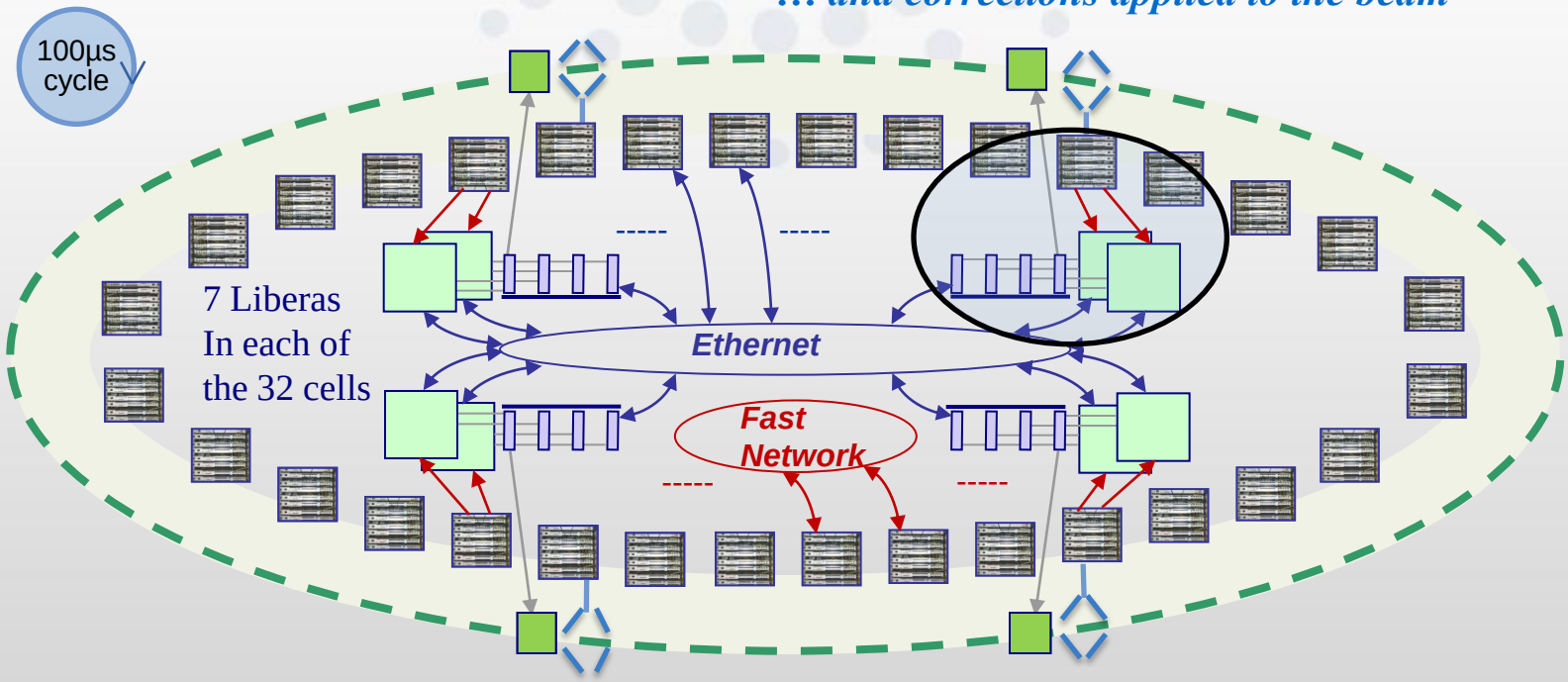
ESRF Fast Orbit Feedback

Fast Orbit Feedback sequencing → *5: Current sent to the correctors…*
… and corrections applied to the beam



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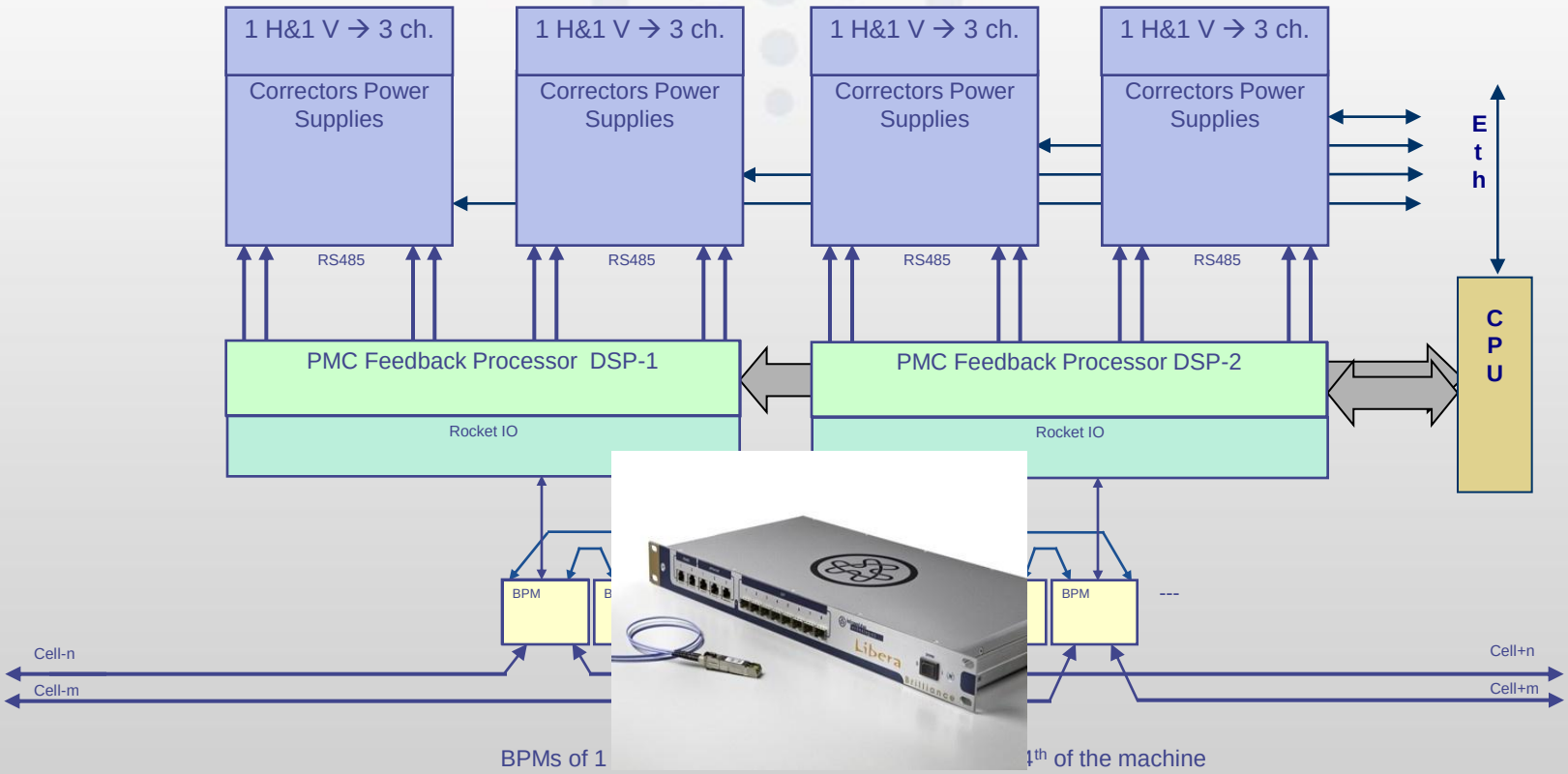
ESRF Fast Orbit Feedback

Topology *(1/4 of the corrections)* ***→ Data from digital B.P.M.s***



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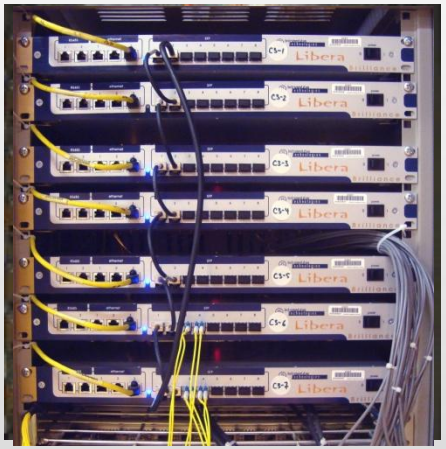
Material involved → Digital B.P.M. Libera Brilliance

Acquisition:

- 224 H & V positions from Libera BPMs grouped by cells (7/cell)
  Position data rate for fast orbit feedback: 10kHz

There are 2 kinds of communication channels:

Configuration, slow rate monitoring	Fast Communication for data exchange at 10kHz
Ethernet	**RocketIOs**



Libera Brilliance. Set-up for one cell

Fast communication: copper for the very short links inside one rack and optic fiber for the inter-cells connections →

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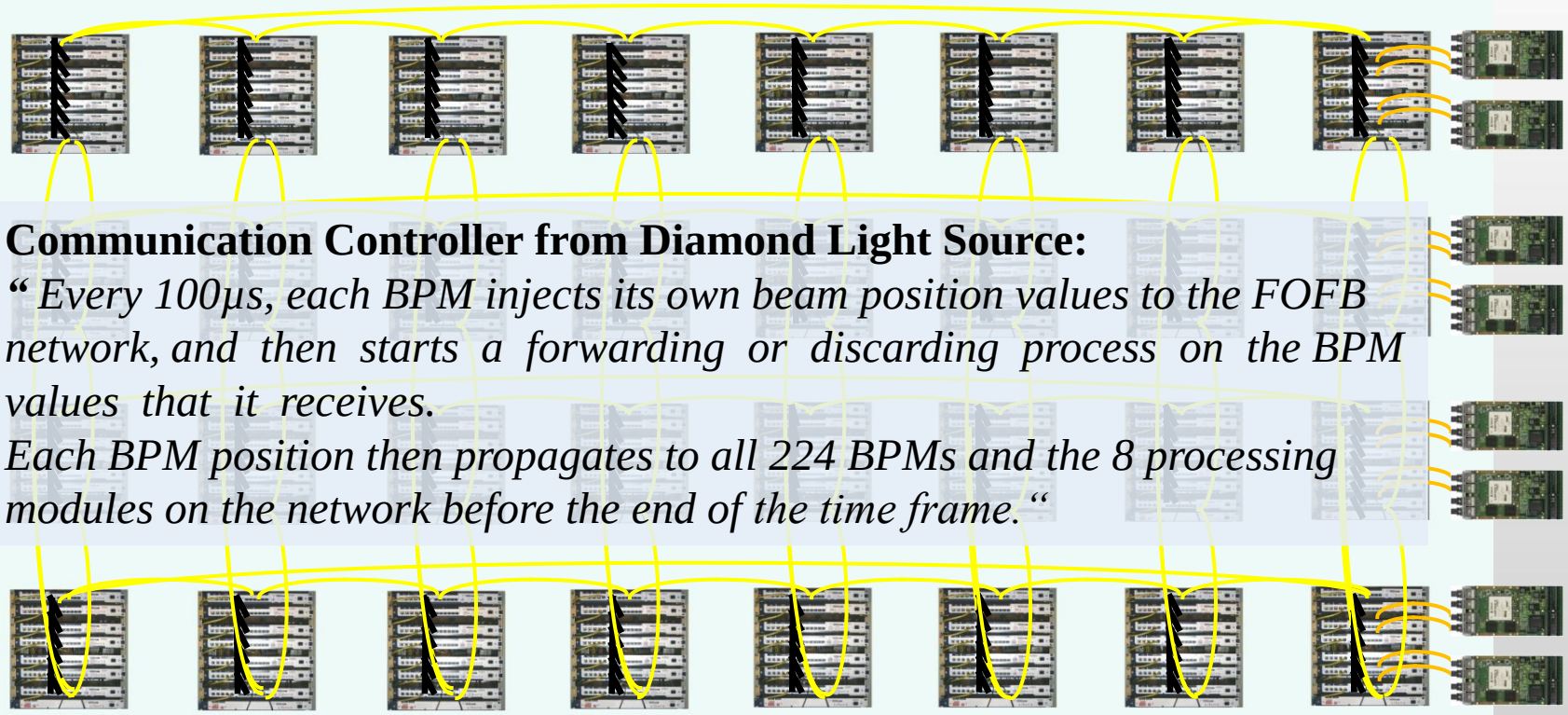
Topology → ***10kHz communication network***



Communication Controller from Diamond Light Source:

" Every 100µs, each BPM injects its own beam position values to the FOFB network, and then starts a forwarding or discarding process on the BPM values that it receives.
Each BPM position then propagates to all 224 BPMs and the 8 processing modules on the network before the end of the time frame."

Libera Brilliance and Digital Signal Processors communication network is redundant

The full exchange of 224 positions H & V should take 50µs even if a connection is broken

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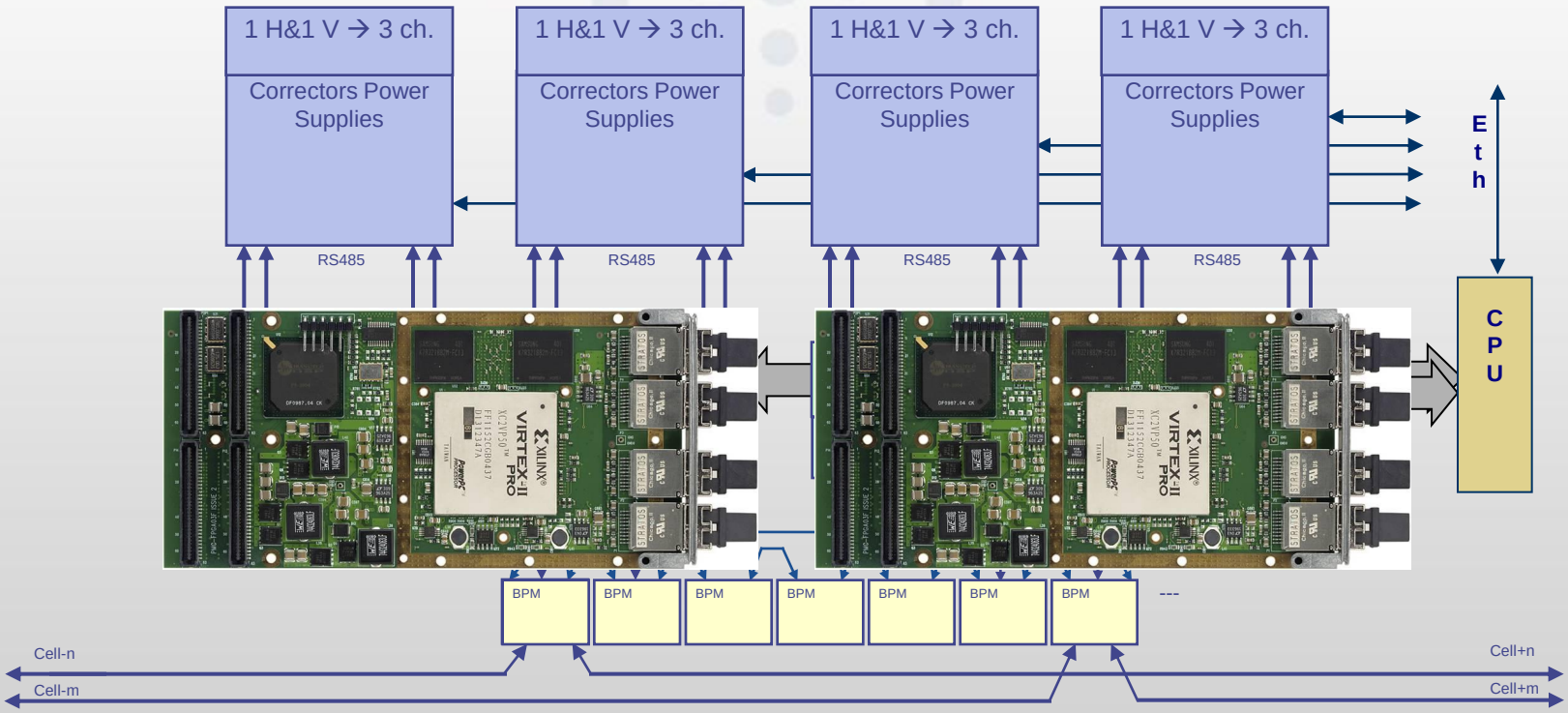
Topology *(1/4 of the corrections)* → ***Digital Signal Processing***



BPMs of 1 cell over 8 and correctors scheme for 1/4th of the machine

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Material involved → ***PMC module (Gbit Ethernet + Virtex-II FPGA)***

- Commercial card in a PCI, same behaviour than Libera (Embedded Diamond L.S. Communication Controller):
  - As communication node and signal processor, the FPGA will embed the signal processing
    → *Real time inside the FPGA*
  - For diagnostic purposes or transfer of parameters through the PCI interface
    → *Not real time*

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ESRF Fast Orbit Feedback

Material involved → ***PMC module (Gbit Ethernet + Virtex-II FPGA)***

- **Digital Signal Processing**:
  - Multiplication by the inverted response matrix,
  - Digital P.I. correction,
  - RS485 Power Converters command.

On an FPGA the computation can be split on many channels running in parallel, the time for computation can be estimated for one channel only:

One compromise between FPGA area occupation and speed can lead to :

224 multiplications + sum, this gives a total of about 300 cycles of the FPGA →less than 3µs

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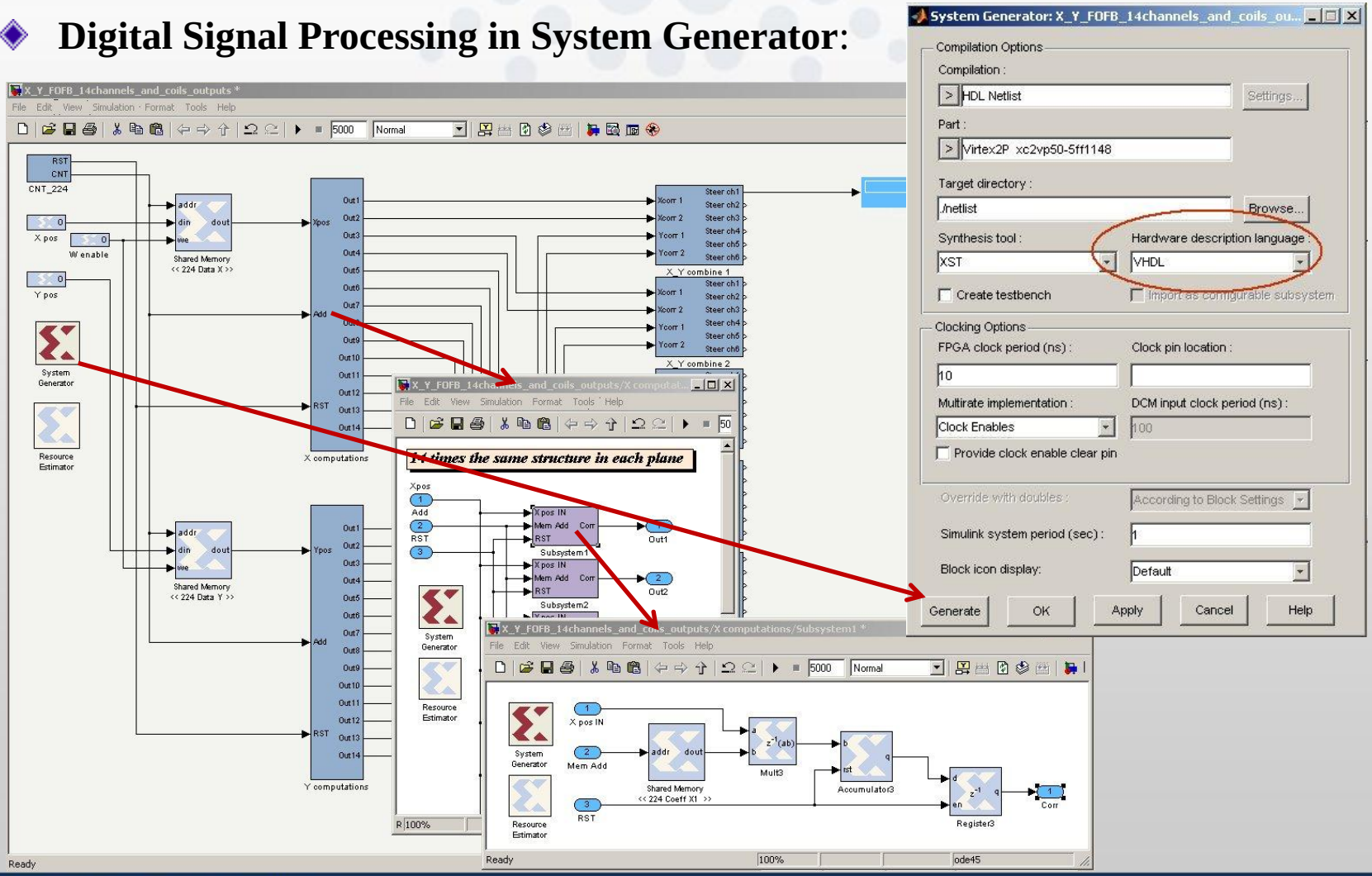
Graphical Programming → System Generator (Matlab / Simulink)

- **Digital Signal Processing in System Generator:**



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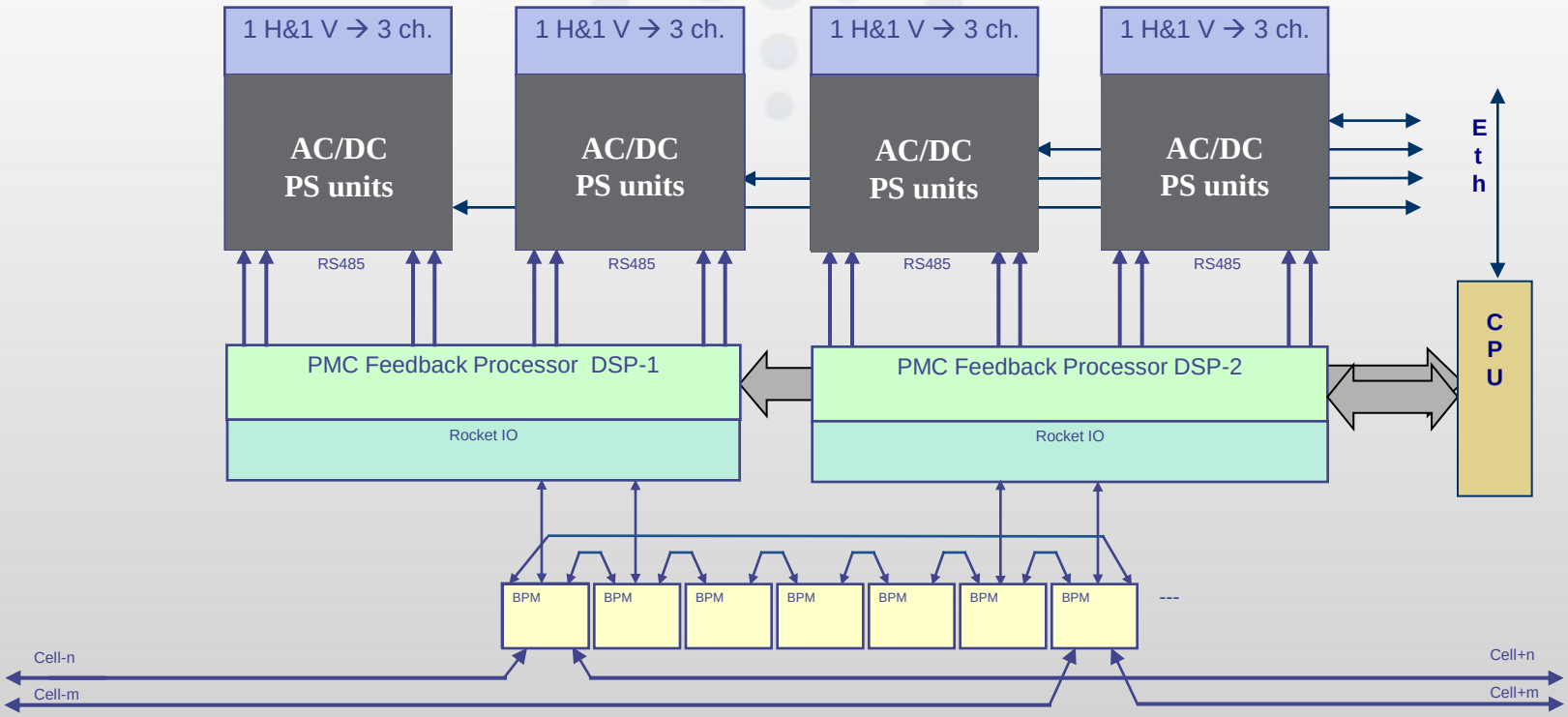
Topology *(1/4 of the corrections)* → ***Steerers Power Supplies***



BPMs of 1 cell over 8 and correctors scheme for 1/4th of the machine

ESRF Fast Orbit Feedback

Material involved

Correction:

- Steerers: 96 Horizontal & Vertical

- Power supplies: 3*96 channels able to drive up to +/- 1.8 Amp DC and up to 0.2 Amp AC *(+/- 15 bits resolution each)*

  288 channels located in 18 cubicles grouped by ¼ of the machine in the technical gallery.

  The corrections will be applied at the acquisition rate, each 100µs.

  A prototype of AC power supply has been validated in real situation.

¼ of the steerers DC Power Converters to be replaced by AC-DC Power Converters

The correctors are part of the sextupoles (6 black coils)

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ESRF Fast Orbit Feedback loop latency

Group delay of FIR:	148 µs	Libera
Group delay of 2 IIR:	<71 µs	Libera
Distribution of data around the ring (DLS C.C.):	50 µs *	Critical inside the 100 µs time frame
Signal processing:	10 µs **	Critical inside the 100 µs time frame
Write into PS controller:	20 µs	Critical inside the 100 µs time frame
Power supply:	70 µs	
Eddy currents in the sextupoles:	75 µs	
Eddy currents in vacuum chamber (stainless-steel):	265 µs	
Total:	<709 µs	

* *Data from Diamond Light Source*

** *Inside the 8 dedicated FPGAs*

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ESRF Fast Orbit Feedback implementation planning

1) Optic fibers for the dedicated network — ***March 2009***

2) Communication Controller on Liberas and one PMC-FPGA processor — ***Spring 2009***

3) AC Power Converter prototype validation — ***Spring 2009***

4) Server for multi-turns diagnostics — ***Beginning 2010***

5) AC Power Converters installed for DC corrections only
(Remote access through Ethernet)
*F*ast correction based on air coil correctors remains active — ***Summer 2010***

1) Implementation of the fast orbit correction on 8 PMC-FPGA processors — ***End 2010***

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ESRF Computing service
ESRF Diagnostic group
ESRF Power Supply group

Thank you for your attention !