Fast Orbit Feedback for DELTA*

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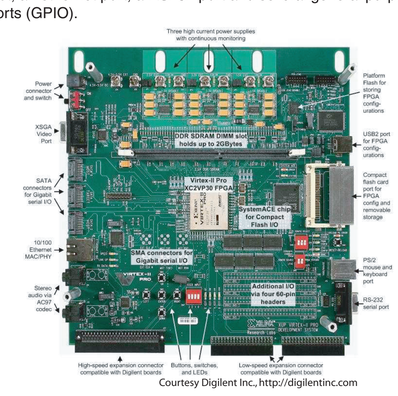
ABSTRACT

The 1.5 GeV electron storage ring at the university light source DELTA suffers from fast orbit movement. Its frequency spectrum points to girder movement, line frequency and its harmonics and the influence of the booster ramp as the source of beam position noise. Fast orbit feedback systems developed at the DIAMOND light source and the Synchrotron SOLEIL ready to cope with this kind of beam noise are based on I-Tech Libera BPM electronics. Based on the XUPV2P FPGA evaluation board we have designed a digital frontend for the Bergoz MX-BPMs employed at DELTA that integrates seamlessly into the feedback loops based on I-Tech Liberas. A fast local orbit feedback has been set up so far. It will be extended to a global orbit feedback in the near future.

MX-BPM FRONTEND

Hardware

The MX-BPM frontend is based on the Xilinx University Program Virtex-II-Pro Development Board (XUPV2P) .
The XUPV2P board is equipped with a XC2VP30 FPGA with 30,816 logic cells and two hardwired on-chip PowerPC processors. Besides other peripherals it provides a DIMM memory slot, a CompactFlash slot, an ethernet port, a RS232 port and several general purpose I/O-ports (GPIO).



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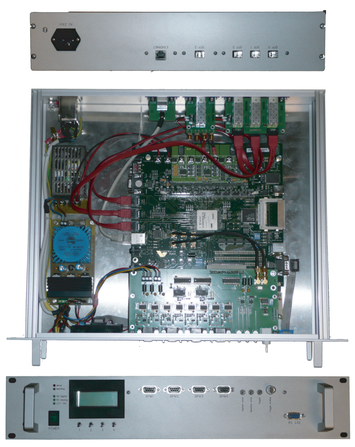
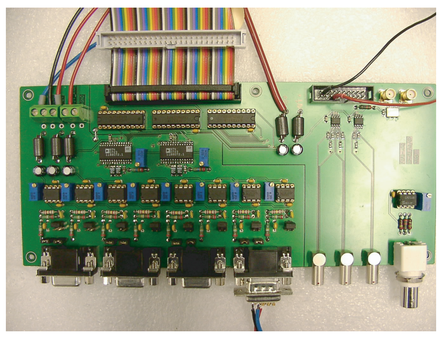


Attached to one of the GPIO ports we developed an ADC-board carrying two Analog Devices AD974 ADCs. Their sampling rate of 200 kSamples/s allows to read the horizontal and vertical beam position data of four MX-BPMs. Averaging over 5 samples increases the precision and reduces the data rate to the desired 10 kSamples/s per channel. The ADC-board also carries inputs for several triggers like the machine clock of the accelerator from which the sampling rates are derived.



The MX-BPM electronics may be clocked up to 40 kHz to obtain a data rate of 10 kHz in the vertical and the horizontal plane. Its analog bandwith should allow a correction bandwith in excess of 100 Hz.

In order to improve the precision of the beam position measurement and to implement a fast global orbit feedback, we have developed a digital frontend for the Bergoz MX-BPMs which provides precision beam position data at 10 Hz to the control system and integrates the MX-BPM seamlessly into the DCC network at 10 kHz data rate.

A FPGA core we call JULIEN, programmed in VHDL handles the ADC board, does the data mining and communicates the measurement data to the DCC and to a read/write FIFO. The DCC has been patched to cope with four BPMs instead of one and is attached to the JULIEN core. It operates the four bidirectional Rocket I/O-ports of the XUPV2P. All four Rocket I/O-ports of the XUPV2P have been routed to SFP jacks that may host either a copper cable connector or a fibre network transceiver.

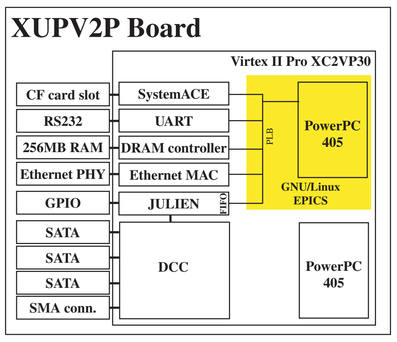
Software

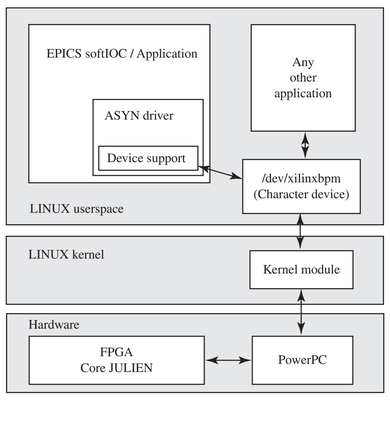
In order to integrate the board into the EPICS control system of the accelerator rings we have installed GNU/Linux on the XUPV2P board.
It is executed by one of the two hardwired PowerPC cores of the Virtex-II-Pro FPGA and uses a 256 MB DDR SDRAM plugged into the board's DIMM slot. Symmetrical multiprocessing of the two available PowerPC cores was not an option because the PowerPC 405 cores do not implement cache coherence.
Peripherals as the UARTLite core for the RS232 console interface, the EMACLite core for the Ethernet PHY and the SystemACE core to access a 2 GB CompactFlash card came with the Xilinx Embedded Development Kit (EDK 10.1.03).
The Linux kernel 2.6.30, equipped with drivers for the XUPV2P board was downloaded and, as well as the EPICS sources, cross-compiled on a x86 host platform using the DENX Embedded Linux Development Kit (ELDK). The hardware bitstream generated by the Xilinx EDK and the ELF-binary of the Linux kernel were then joined together and installed on the first partition of a CompactFlash card, while the root file system, based on Busybox, was installed on the second partition.
The board is booted from the CompactFlash card. The FPGA bitstream is loaded into the FPGA fabric before the kernel code is executed. Thus, all peripheral devices necessary for Linux are present at boot time.

The data exchange between the JULIEN core and the Linux user space is realized by a kernel module providing a character device. The module detects the core, mapped into the memory by the kernel, and reads data from it over a read/write FIFO.

Even though we do not use any real time patches to the Linux kernel, more than 10^5 data frames of 192 bit length can be read from the FIFO at 10 kHz frame rate before the first data frame is lost.
Reading the data of *all* BPMs in the ring, present at every 10 kHz time step in the DCC, cannot be done this way. On the long run we plan to implement Direct Memory Access for a sniffer board in order to obtain this data.

After the Linux system is up, an EPICS softIOC is started. Communication between the kernel driver and the EPICS record was programmed using the asyn-driver framework. The device support reads averaged BPM data at 10 Hz frame rate and distributes it over the machine network.



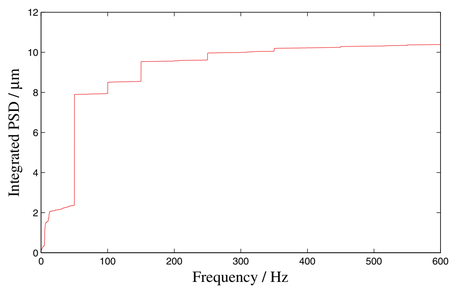


Measurements

The core's access mode can be chosen by writing to a register in the core. In fast access mode, the core writes data frames of 192 bit length at a rate of 10 kHz to the FIFO. Besides frame number and markers they contain raw ADC values for both the vertical and the horizontal plane of all four BPMs. In slow access mode the module asks for a sum of N readings ten times a second.

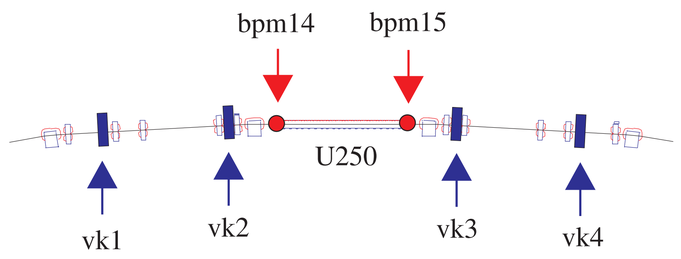
The avaraging lenth N may be up to 16384, corresponding to an averaging time of approx. 1.64 seconds. The data frame in slow access mode is thus almost twice as long (320 bit instead of 192 bit) as in fast access mode. The slow data has, due to averaging, a higher precision. We have measured rms errors of the mean at N=1000 (Bandwidth=10Hz) of less than 400 nm.

The integrated power spectral density (PSD) of the beam movement in the storage ring, measured using the MX-BPM frontend is shown in the figure.

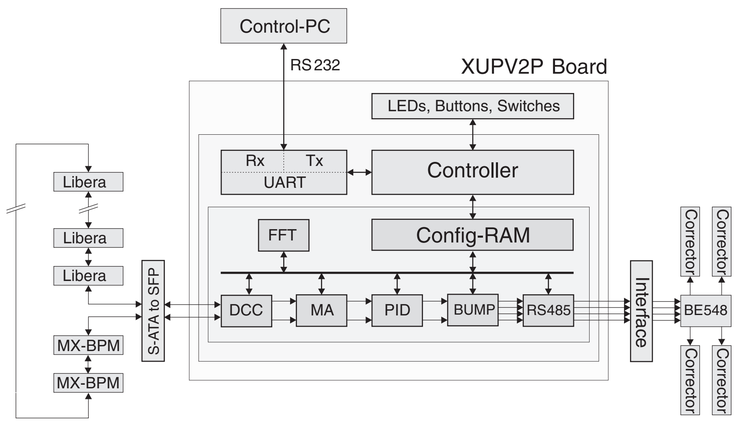


LOCAL ORBIT FEEDBACK

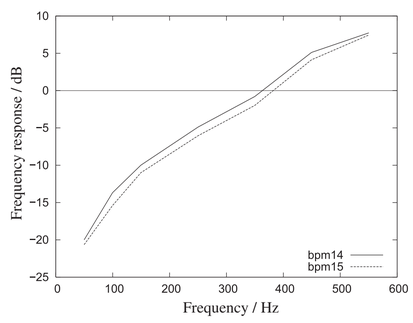
As a proof of concept we have implemented a vertical local orbit feedback in the FEL undulator section of the storage ring. We used two I-Tech Libera BPMs and four vertical correctors for the feedback, while five spectator BPMs distributed around the ring measured the feedback's impact on the remaining machine.

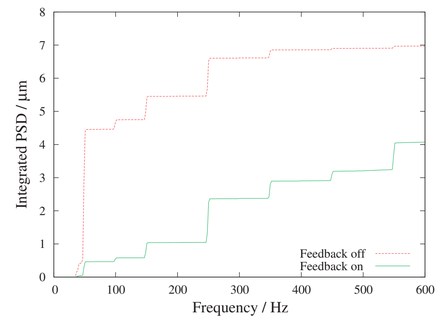


In this setup the XUPV2P was employed to receive the BPM data over the DCC network, calculate the orbit correction using a SVD-inverted response matrix prepared beforehand and apply the correction over a PID controller to fast power supplies. This part of the software ran entirely in the FPGA. A link to the control system was not implemented.



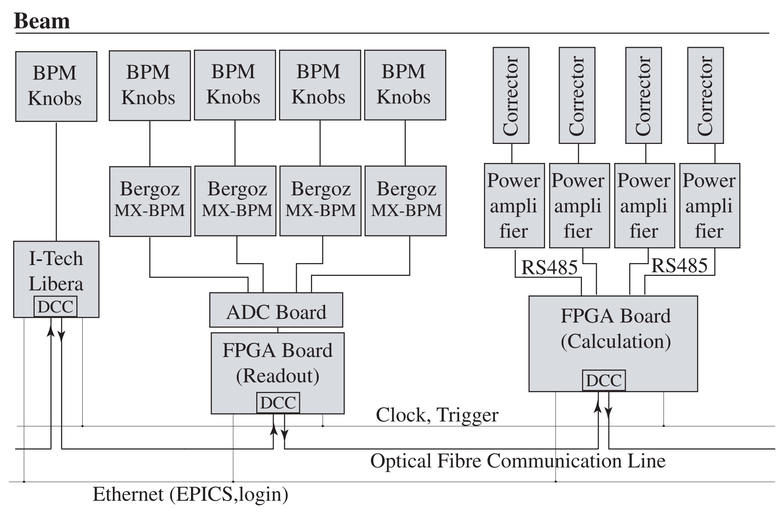
After optimizing the PID controller parameters, we achieved a damping of the 50 Hz line frequency of -20dB. The bandwidth of the correction was limited to approx. 350 Hz. In order to compare BPM capabilities, as the next step we will replace the two Libera BPMs by Bergoz MX-BPMs and XUPV2P boards and repeat the same measurements.





FUTURE GLOBAL ORBIT FEEDBACK

The figure below shows a sketch of the future global orbit feedback planned for the DELTA storage ring. Libera BPMs and Bergoz MX-BPMs will send BPM data frames at a rate of 10 kHz into the DCC network while XUPV2P boards pick up the data, calculate corrections and apply them to fast corrector power supplies.



Up to now, all parts of the software have been programmed at least as proof of concept implementations. We plan to equip all MX-BPMs during the winter shutdown with digital frontends and run them in parallel to the existing system. After careful checks we plan to switch completely to the new system in spring 2010. The magnets for the fast feedback will be installed thereafter so that we hope to commission the fast feedback system in summer 2010.

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