FPGA Digital Timing System for Fusion Plasma Diagnostics in LHD

Nakanishi H., Ito Y., Kojima M., Ohsuna M., Imazu S., Nonomura M., Nagayama Y., Kawahata K., Sudo S.

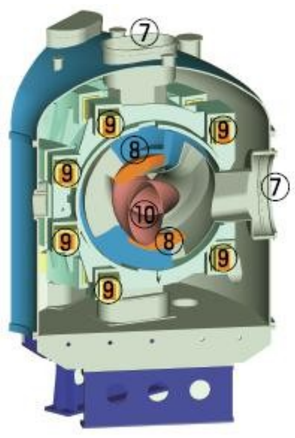
National Institute for Fusion Science (NIFS), 322-6 Oroshi-cho, Toki 509-5292, Japan

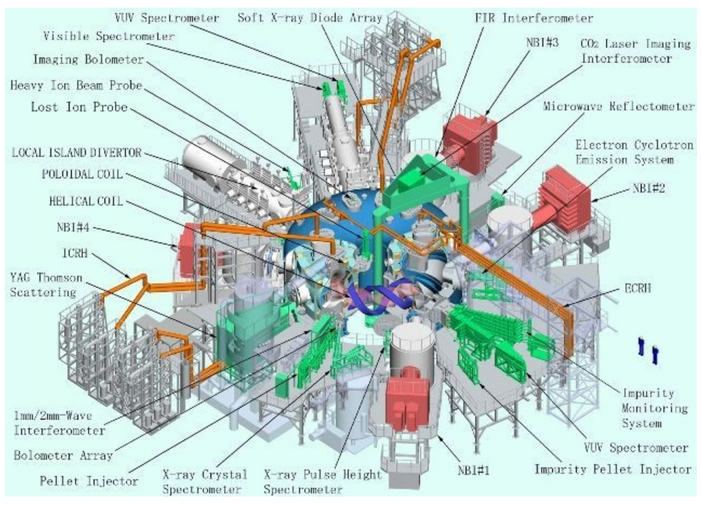
1. Large Helical Device (LHD)

The Large Helical Device (LHD) project has involved the construction of the world's largest superconducting helical device, which employs a helio-tron magnetic field originally developed in Japan. The objectives are to conduct fusion-plasma confinement research in a steady-state machine and to elucidate important research issues in physics and engineering for helical plasma reactors.

The LHD comprises a plasma confinement device that employs superconducting coils, plasma heating systems and devices to measure and record plasma properties and phenomena. Many (~70) types of diagnostic devices are used to measure high temperature plasmas in the LHD. These are used to investigate a wide variety of plasma characteristics. Measurement by multiple devices improves reliability of information about the space and time variation of plasma parameters.

Outer diameter	13.5 m
Toroidal plasma diameter	~ 8 m
Poloidal plasma diameter	1.0 ~ 1.2 m
Magnetic field Bo/Bmax	3/6.6 T
Helical pitch No. l/m	2/10
Net weight	1500 t



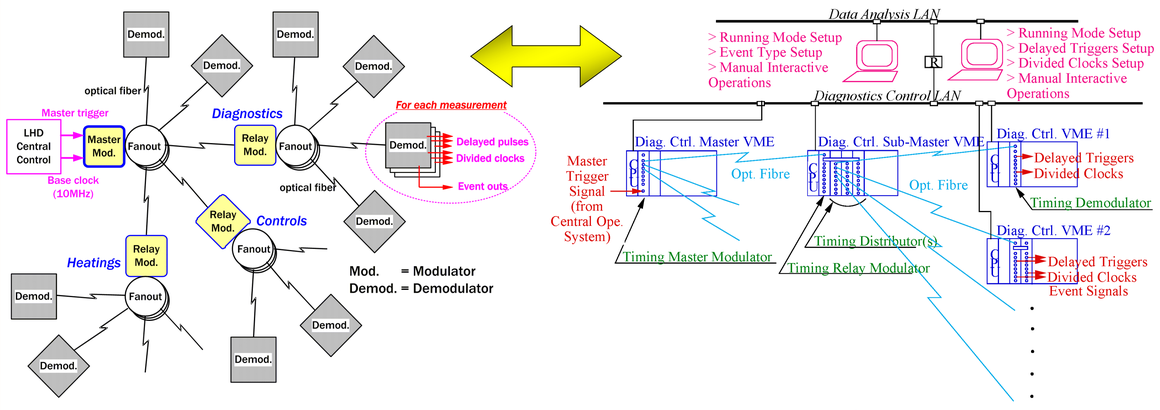


Figures: LHD parameters and plasma diagnostics

⑦ Diagnostic ports
⑧ Superconducting helical coils
⑨ Superconducting poloidal coils
⑩ Plasma

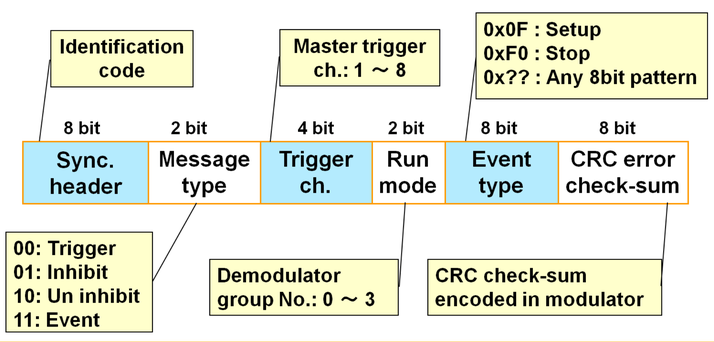
2. Background

To supply the various digitizers with their own start trigger and sampling clock independently, we developed the digitally synchronized timing delivery system (DTS) for LHD fusion plasma measurements more than 10 years ago. It is a synchronous clock and trigger distribution mechanism whose tree-structured optical fiber links connect the **single master modulator** and **terminal demodulators**.



Figures: Modulator-Demodulator chains in logical & physical views

As those modules were made based on VMEbus standard and running on VxWorks RTOS, all the master and terminal nodes need their own cpu board, vme backplane and chassis. Their hardware and software maintenance or improvement, therefore, have needed high expenses including the development environment and license.



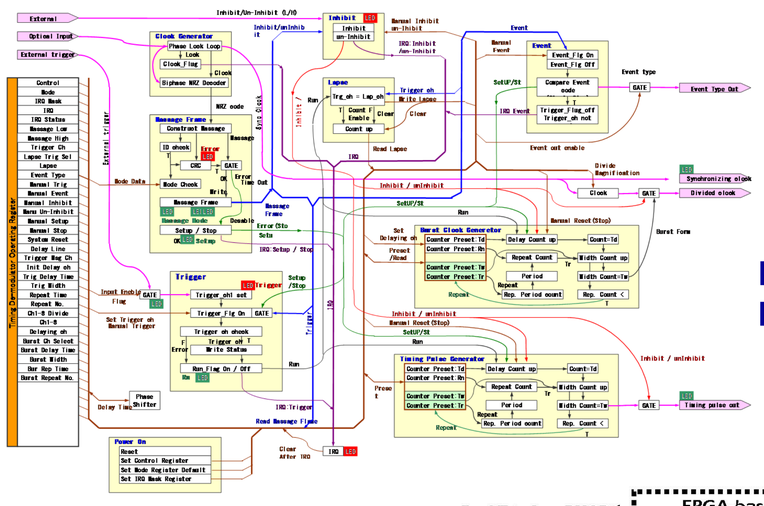
Figures:
32-bit timing message frame distributed from Mod. to Demod., always sent 3 times consecutively

3. New "SoC"-based DTS Implementation

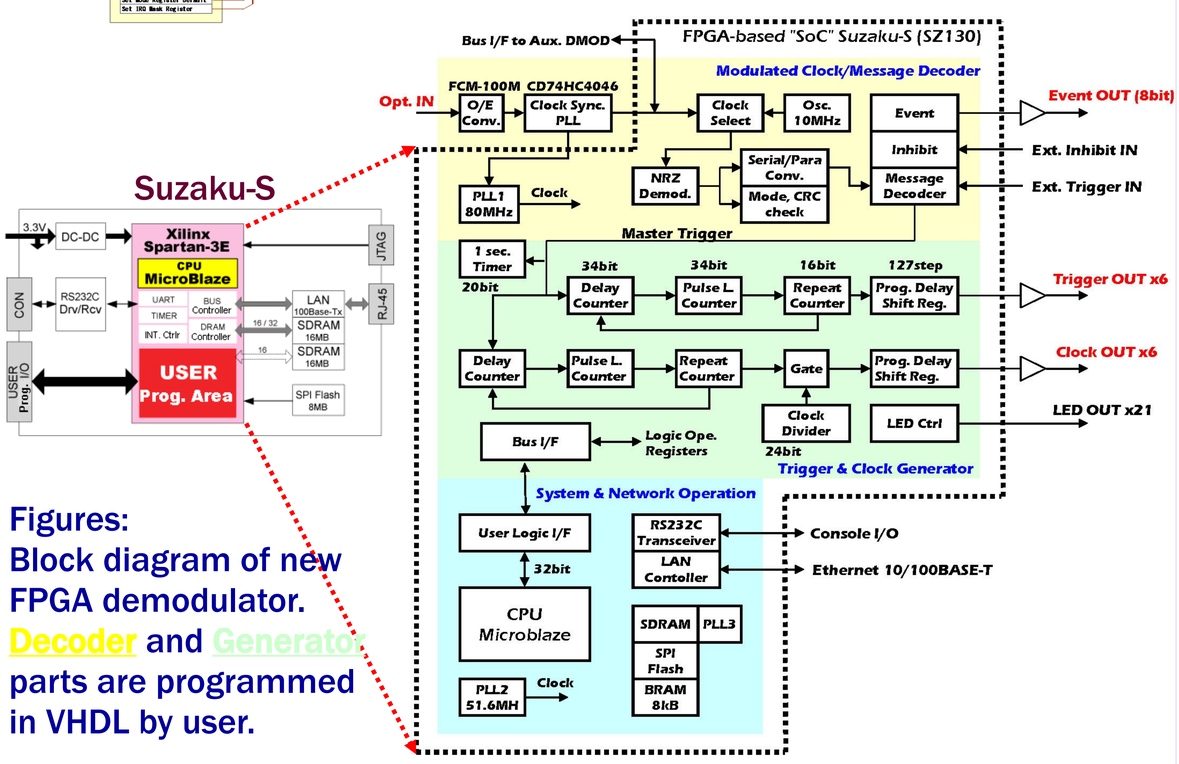
Required conditions:

1. As DTS demodulator uses many 16 or 34 bit counters in logics, the required number of gates should be more than a million. Chip cost is another important issue.
2. To port the VxWorks-based onc-rpc server codes, the SoC should include a cpu core on which any linux/unix-like OS runs to execute them.

We have chosen a semi-finished FPGA-based module **Atmark Techno's "Suzaku-S (SZ130)"**, which has a 1.2Mgate Xilinx Spartan-3E FPGA chip on board and a software processor Microblaze can be embedded within it. As it costs only about us$ 300 having card-size (47*x*72 mm) dimensions, we have decided that it is quite suitable both in casing and mass use in LHD.



Figures: State chart of DTS Demodulator



Figures:
Block diagram of new FPGA demodulator.
Decoder and Generator parts are programmed in VHDL by user.

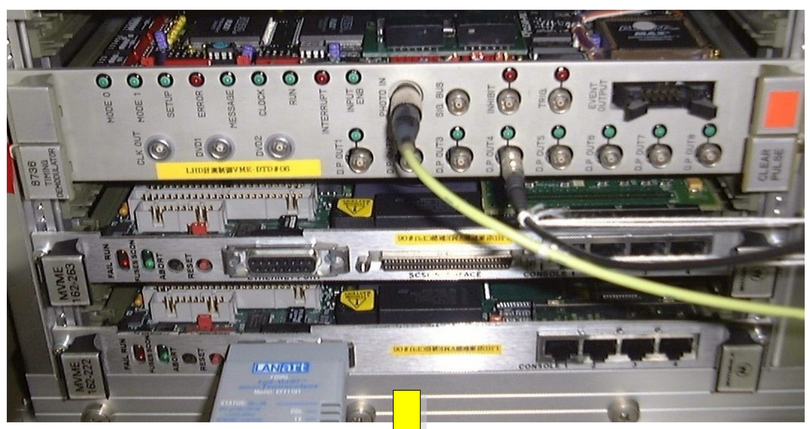


Figure:
Old VME/VxWorks DTS ported to FPGA/ μCLinux "SoC"; Suzaku-S (SZ-130)

5. Results & Conclusion

First, we developed a prototype having 8 triggers and 8 clocks with the gated outputs. Then, the logics spent 80~90 % of silicon resources in which the timing counters are widely arranged on logic area and therefore the cpu region was somewhat restricted. In such the situation, cpu could not boot at the optimal clock of 51.6 MHz. To recover this problem for practical use, we have lessen the number of implemented trigger and clock/gate channels from 8-8-8 to 6-6-6, and also reduced the cpu clock from 51.6 MHz to 36.8 MHz for the stability margin.

The new FPGA demodulator is fully compatible with the former optical links and also tcp/ip communications so that we can use old and new demodulators mixed without any change. The cost advantage of the new unit is remarkably one-tenth the original VME one. It consumes only 1.2 W electric power, and thus will be a very reliable maintenance-free box without any cooling fans. As this semi-finished SoC platform is very useful to homemade an intelligent digitizer unit, another fast latching scaler (photon counting) module is now designed for LHD.