Single Board Computer for device control in the FAIR accelerator control system

M. Thieme, W. Panschow, S. Rauch, M. Zweig

GSI Helmholtzzentrum für Schwerionenforschung GmbH, Darmstadt, Germany

Abstract

For the FAIR accelerator control system a new single board computer (SBC) is presently under development. The SBC will be the core of the distributed intelligent peripherals and shall be realized as a multi-controller system, consisting of up to three controllers. The main components of the SBC are a powerful FPGA and a highly integrated computer-on-module (COM). FPGA and COM communicate via PCI or PCI express. With use of the COM the performance of the SBC gets flexible and scalable. If needed, the COM can be upgraded. For the communication with the controlled devices several interfaces are foreseen: A parallel bus interface, an up to 32 bit wide uni-/bidirectional interface and up to four serial high-speed links (>500 Mbit). Up to three Ethernet interfaces (100/1000 Mbit) are provided for the user interface to the higher control layers and general machine timing system. For diagnostic purposes the SBC holds USB, EIA-232 (RS-232) and JTAG (IEEE 1149.1).

Introduction

For the new accelerator complex FAIR (Facility for Antiproton and Ion Research) at the GSI Helmholtzzentrum für Schwerionenforschung GmbH, a control system in 3-tier architecture with local intelligence will be put into use.

Different to the existing control system of the accelerators at the GSI, where the control of the client devices is done with a field-bus system, the control system for the FAIR-Accelerator shall be equipped with IP-communication on Ethernet basis.

A fundamental portion of the local intelligence will be provided by a dedicated front-end controller. Power Supplies, RF-Systems, Kickers and others will be fitted with this as intelligent IP-Node(See Figure 1).

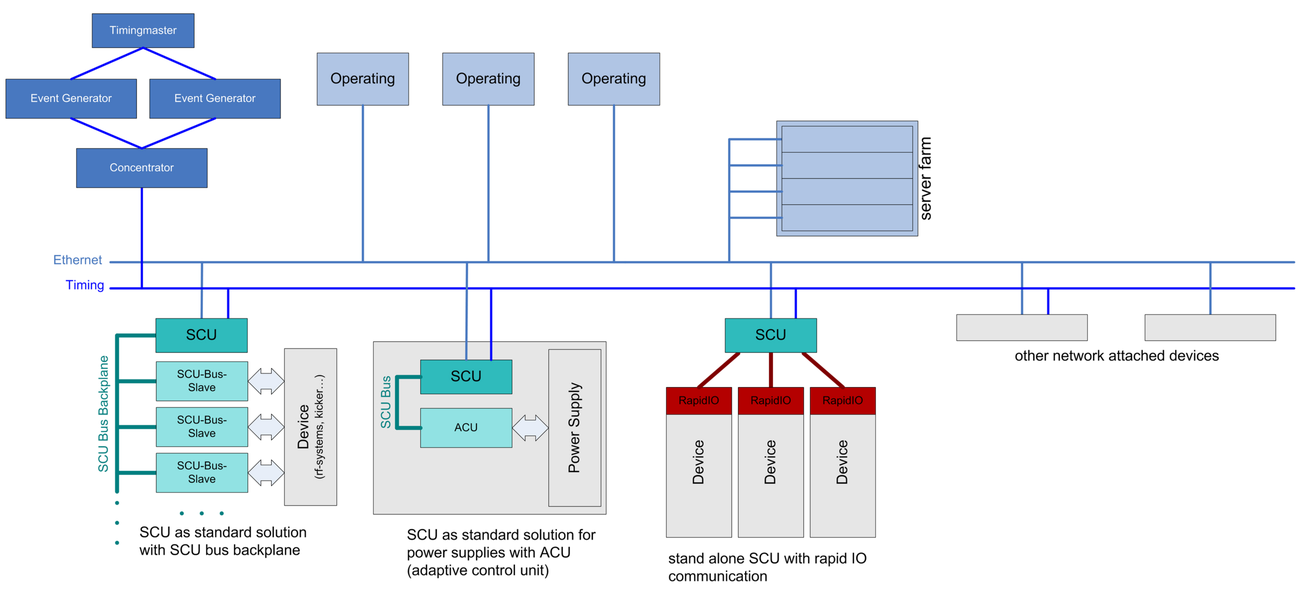

Figure 1: SCU-Integration in the accelerator control system

From this the challenge arose of finding a solution for a suitable front-end controller. There it was necessary to fulfill the following specifications at minimum:

- IP-Communication over Ethernet; via copper or optic fiber
- Provision of a robust, adequately fast, and simple to use local interface for attaching the client devices and client device specific components (ADC, DAC, digital I/O, pulse generators, DDS, counters, etc.)
- Size of assembly according to the 19-inch racks with a unit height of 3 U
- Long term availability of the used electronic components and second source
- Ease of service and maintenance; diagnose from afar, firmware and software updates via Ethernet
- Abdication of forced air cooling
- Ease of expandability and the option of adjustment to higher requirements regarding performance
- IP link to Ethernet based timing system
- Ability to run Linux as operating system

These specifications shall be met by the "SCU - Scalable Control Unit" named controller, which currently is under development.

Block Diagram

The main components of the SCU controller are a COM Express™ module and a powerful FPGA(See Figure 2).

The module will be mounted on a carrier board (Eurocard) which provides the physical interface to the periphery. The COM Express™ module uses a Gigabit Ethernet Channel and USB for external communication. With the FPGA another Gigabit Ethernet channel, a USB interface, a proprietary parallel bus, an interface for client devices and client device specific components, two serial high-speed channels, and general purpose I/O are provided by default.

By operating the COM Express™ module the SCU can provide the resources of a complete PC. Reasons for choosing a COM Express™ module as core are as follows:

- The modules have a standardized interface for system integration
- The tight construction and standardized form factors simplify the constructional solution.
- There are different processors available, beginning with the very low power Intel Atom to the high performance Intel Core2 Duo with different clock frequencies and arbitrary memory size.
- There are many suppliers of these systems, so that the availability is ensured for the near future.
- As off-the-shelf product for industrial use it will be produced in large quantities, is easily available and cost-effective.
- We can follow the update cycles of the chip production and the chip technology without redesigning the SCU carrier board.

All this reasons lead us to refrain from the development of a CPU core of our own.

Mainly due to the COM Express™ module we achieve a scalability of the SCU. On the basis of needed processing power and memory requirements a respective module can be chosen.

As standard solution the SCU are equipped with Intel Atom. With that CPU there is no need for a forced cooling within the unit.

The FPGA had been chosen in a way that in case of need up to two controllers can be implemented. Standard is one controller. Using an extension board the SCU will optionally be able to provide an additional Gigabit Ethernet channel, additional serial high-speed channels and auxiliary digital I/Os. Respectively the carrier board features an expansion slot.

For commissioning, service and diagnostics, USB, EIA-232(optional) and JTAG (IEEE 1149.1) are available.

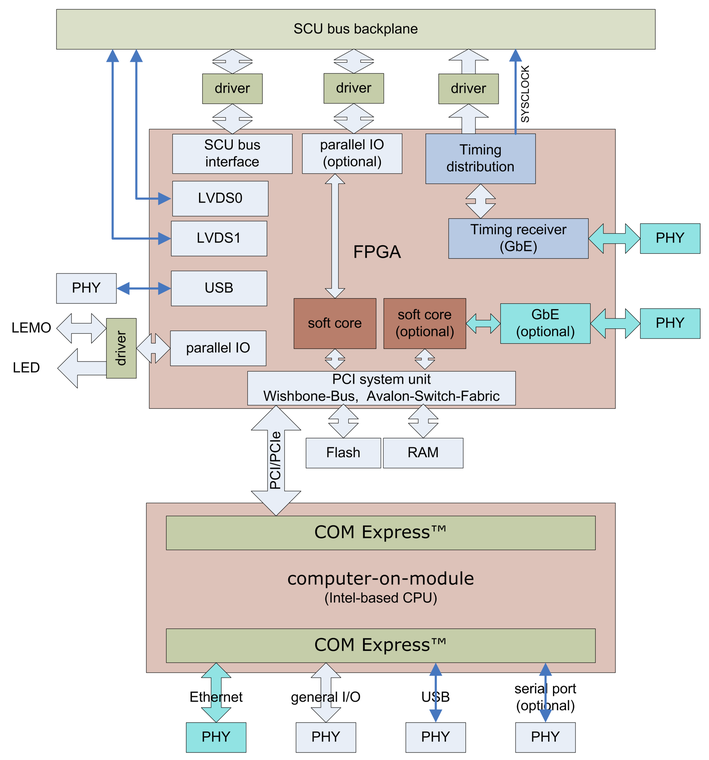

Figure 2: Block diagram of SCU

Distributed Processing

The control system software runs under Linux on the CPU of the COM Express™ module. For time critical functions, the FPGA is available. Thus it is possible that functions are realized directly on hardware level (VHDL).

An example is the hardware-implemented function generator with optional linear or quadratic interpolation.

Other functions, e.g. for signal recording (soft-scope), are realized by hardware (VHDL) and software (soft core).

The local Parallel-Bus-Interface

For means of communication between the SCU and the client devices, as well as client device specific components a local parallel bus is used. This so called SCU Bus is a proprietary solution which will be used for the control system of the accelerator complex FAIR and in future for the existing accelerators of the GSI too.

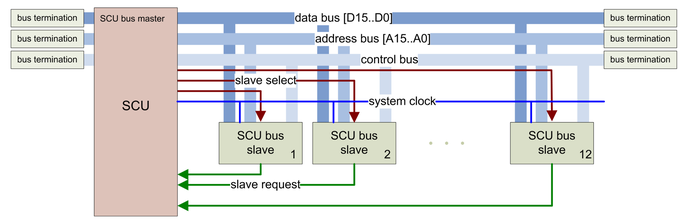

Figure 3: Master-Slave architecture of SCU-Bus

The SCU bus utilises master-slave architecture. There is a bus master, the SCU and up to 12 slaves(See Figure 3).

This simple parallel solution has the advantage that the bus interface is designed in an uncomplicated manner and can be realized with a small and cost-effective FPGA or EPLD. The complete bus interface including the arbitration will be provided as a VHDL macro and can be used on client device specific components (SCU bus slaves).

Next to the normal data traffic between SCU and SCU bus slaves, the SCU bus distributes timing information. This timing information is synchronized throughout the system. Read-Write-Cycles of the normal data traffic run event-driven and asynchronously concerning the timing.

The SCU accordingly processes a system-wide master clock and provides it on the SCU bus.

Form factor and mechanical setup

By using the COM Express™ module in conjunction with the highly integrated FPGA, a very compact assembly is achieved.

- The carrier board of the SCU is built as a Eurocard 100 mm x 160 mm.
- The SCU is mounted in a casing of 14 HP widths(See Figure 4).
- The assembly is made to be able to refrain from forced cooling.

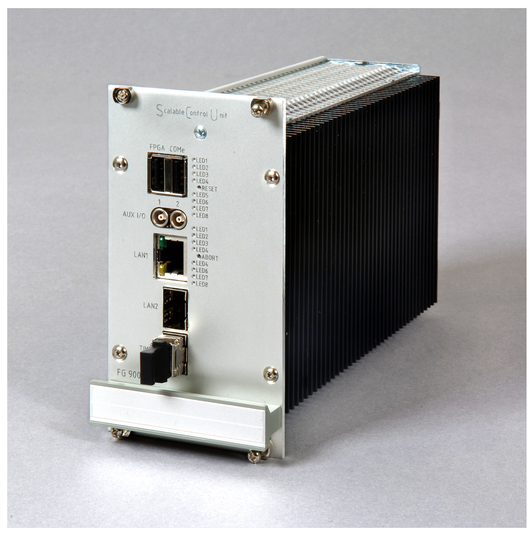

Figure 4: Mechanical model of the SCU

Optionally the casing can house an extension board, which provides additional Gigabit Ethernet channels, additional serial high-speed channels, auxiliary digital I/O's and further functions.

As standard solution, the casing is mounted together with the SCU bus in a 19-inch rack or directly within the respective assembly group carrier in the client device (mostly power supply units).

If needed the SCU can be run stand-alone without the SCU bus. In this case, the SCU bus interface only provides the power supply. The communication with the client devices then uses the serial high-speed channels.