Development of a New Control System for the FAIR Accelerator Complex at GSI

R. Bär, U. Krause, V. Schaa, M. Thieme, W. Schiebel
GSI Helmholtzzentrum für Schwerionenforschung GmbH, Darmstadt, Germany

Presentation TUP107

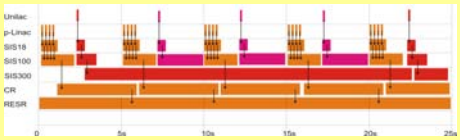
Abstract

The 'Facility for Antiproton and Ion Research' (FAIR) will be realized at the 'GSI Helmholtzzentrum für Ionenforschung GmbH' (Darmstadt, Germany) in the scope of a large international organization. This new accelerator complex will be a significant extension to the existing GSI accelerator chain. It will present unique challenges for the control system which are well beyond the capacity of the present system. A new control system is under development that considers all aspects of the expected functionality to operate the GSI/FAIR machines and integrates the present GSI controls infrastructure. The new control system substantially builds on proven principles and solutions and is based on a strictly modular design with well defined interfaces. Size and organizational structure of the FAIR project with international contributions demand for a high level of standardization and efficient interface management. This report summarizes concepts, architecture, technologies and building blocks of the new system.

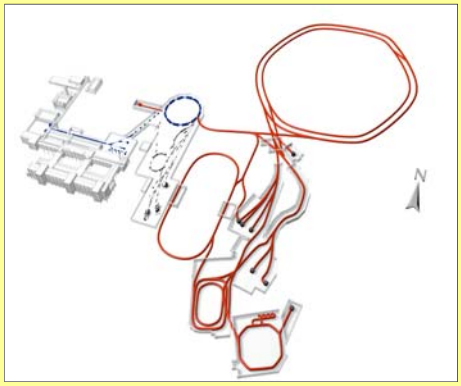
The FAIR Accelerator Complex

The Installation
- up to nine new accelerator installations
- built in several stages
- existing facility is upgraded and acts as injector
- increased complexity, e.g. massive parallel operation

The Project
- official launch of the FAIR start version: November 2007
- staged realization for cost overrun reasons
- start of construction works expected in fall 2010
- commissioning of the first FAIR systems expected for 2015



Parallel operation in the FAIR complex


FAIR facility overview

Control System Design Considerations

Present CS well adapted to present needs but...
FAIR challenges are well beyond the present system capacity:
- timing precision and parallel operation
- overall machine and operation complexity
- scalability, data acquisition performance
- superconductivity and safety functions

Further boundary conditions
- limited resources: manpower, costs
- tight time schedule, several years of commissioning
- involvement of partners
- integration and maintenance of existing injector chain

Design Considerations
- strategy of CS implementation has to be most effective
- strict strategy of standardization (interfaces, sw developments)
- provide development frameworks and workflows for developments

Control system design
- not fully done yet, presently detailed technical design phase
- decentralized, distributed system
- strictly modular design, break in work-packages
- based on Linux OS, C++ and Java
- build substantially on proven principles and solution of the existing control system
- investigate best practices of other solutions, identify and adopt proven solutions as CS building blocks to reduce dev. effort

Collaborations
- CERN and FAIR have similar controls requirements
- several fields of collaborations have been identified
- collaborations started on FESA, LSA, Timing (other on the horizon)

FAIR controls development concentrates on
- particular solutions (e.g. standard FE controller SCU)
- missing functionality
- integration of existing controls stack
- integration, adaptation and extension of controls building blocks

Front-End Software Architecture

Central part of the FAIR control system

FESA (Front-End Software Architecture)
- developed by CERN
- working solution for LHC and injectors
- equipment control and DAQ system
- software framework provides full environment and tools to design, develop, implement, test and deploy device software
- design objectives: standardize, speed-up and simplify the task of FE software development

Main reason to adopt
- high level of maturity
- system is available NOW
- specs for FE systems and training of staff/partners can be started early in the project

Active and fruitful collaboration between CERN and GSI
- presently development of FESA v3 (complete redesign)
- generic functionality in base, laboratory packages
- avoid code branching, g necessary in the
- FESA device class developments at GSI

Setting Generation and Management

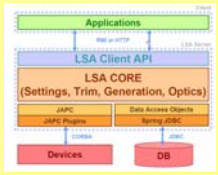
Presentation THP012

Central part of the FAIR control system
Active and fruitful collaboration between CERN and GSI

LSA (LHC Software Architecture)
- developed by CERN (2001), generic objectives
- working solution for settings management and data supply
- provides very generic solutions, easy re-used and extended for FAIR
- provides interface for applications to access accelerator data
- written in Java using Spring framework

- accelerator is modeled by describing parameter hierarchy
- enables machine physicists to implement machine model

Present activities
- model existing SIS18 synchrotron for further evaluation, then SR
- extend LSA for GSI/FAIR and future CERN needs
- implement modeling of accelerator chains



LSA software stack


Example of LSA parameter hierarchy (from physics to settings)

Dedicated Equipment Device Controller SCU

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Development of a custom and cost-effective solution for FE equipment control

- about 1500 units in FAIR for power converters, rf-systems, etc.
- integrated in equipment (e.g. power converter cabinet)
- form factor / bus system evolution for compatibility/upgrade

- highly integrated computer-on-module (COM Express module)
- powerful FPGA for time-critical functions (e.g. timing receiver, FG)
- primary interface: 32-bit wide bidirectional parallel bus
- option: high speed serial connectors (>500 MBit)
- 3 Ethernet connectors (communication, Timing)

- FE software runs under standard Linux OS; FESA
- time critical functions are realized directly on HW level (VHDL)

Activities:

- technical evaluation: PCIx communication tests, thermal tests, etc. no showstoppers so far

- design of the PCB for the FPGA carrier board

- first full complete unit is expected to be tested in the lab by mid 2010.


mechanical model of the SCU device controller

Timing System

A new timing system is developed for the GSI/FAIR complex

Requirements:
- compensate signal transmission time
- provide absolute timestamps for distributed systems
- transmit events
- reverse communication channel (bidirectional communication)

Solution:
- dedicated timing network, tree topology
- use Gigabit Ethernet as transmission technology (Cu, fiber)
- implement "White Rabbit" protocol
- develop WR enabled devices (switch, master, receivers)
- implement forward error correction algorithms for robustness

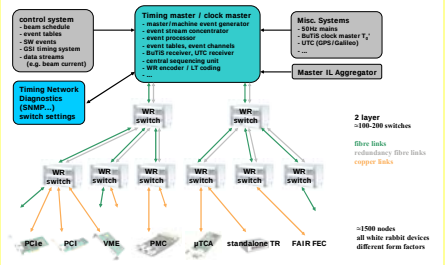
White Rabbit?

Presentation WEP029

- low level timing and control transport protocol
- use Synchronous Ethernet standard
- use Precision Time Protocol standard
- implemented on OSI level 2
- provide reliable and deterministic transmission channel

Collaboration with CERN and other institutes

FAIR Timing System Architecture



timing event messages
granularity windows concept